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Filed: 12/15/2003

## REMARKS

Prior to the foregoing amendments, claims 1-35 were pending in the application. With the addition of new claim 36, claims 1-36 are currently pending.

On or about July 21, 2006, the Examiner required restriction among the originally filed claims, asserting that the claims were restrictable as follows:

Group I including claims 1-8 directed to a mask set,
Group II comprising claims 9-18 directed to a method
of making a planar circuit using a mask set of Group I,
Group III comprising claims 19-34 directed to a
planar circuit made using the method of Group II.

In a response dated on or about August 21, 2006, applicants elected the Group I claims and added claim 35. The election was with traverse.

In the office action dated October 4, 2006, the Examiner acknowledged that claim 35 should be grouped with Group II and made the restriction requirement final.

Applicants respectfully request reconsideration of the restriction requirement. Claims 9-36 have been withdrawn from consideration by the Examiner but have not been cancelled in view of this request for reconsideration.

New claim 36 has been added which applicants believe belongs to the Group I claims. Claim 35 has been amended and now belongs to the Group I claims. Amendments to claims 9-18 and 19-34 have been made in order to more expressly link claims 9-34 to the Group I claims.

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Accordingly, applicants respectfully request that the restriction requirement be withdrawn as to the amended claims and that all of the claims currently not cancelled from the application be addressed and examined by the Examiner in this application.

Reconsideration of this application in light of the foregoing amendments and following remarks is respectfully requested.

Claim 1 has been rejected under 35 USC § 102(e) as being anticipated by Roberts (6,517,997). This rejection is respectfully traversed. Claim 1, as originally filed, specifies that the first pattern includes a featureless region disposed therein such that the planar circuit is incomplete.

Roberts does not disclose providing a featureless region disposed such that the planar circuit formed is incomplete. In fact, Roberts teaches away from the invention defined in originally filed claim 1 by providing a featureless area that provides optical communication between first and second areas of an optical device (i.e., that completes the planar circuit). Accordingly, it is submitted that independent claim 1, and claims 2-8, which depend from claim 1, are novel.

Claims 1-8 have been rejected under 35 USC § 103(a) as being unpatentable over Roberts (6,517,997) in view of Fritze et al (6,818,389) and Liu (7,082,596). Claim 1 has been amended to specify that the planar circuit is a planar lightwave circuit. It is respectfully submitted that it would not be obvious to one having ordinary skill in the art to take

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the teachings of Roberts and combine them with the teachings of Fritze et al. or Liu, in order to make the invention defined in amended claim 1, because Roberts teaches away from it. In particular, the focus of Roberts' application is to avoid stitching patterns where waveguides meet (e.g., see column 1, lines 60-67 and column 2, lines 1-7) by using a mask set that overlaps in a featureless region of the planar lightwave circuit. In the invention defined in amended claim 1, features of the second pattern are used to complete the planar lightwave circuit (i.e., in direct contrast to the featureless region disclosed in Roberts). Accordingly, it is submitted that amended claim 1, and claims 2-8, which depend from amended claim 1, are allowable.

In addition, the rejection of original claim 2 is respectfully traversed. First of all, it is respectfully submitted that no combination of the references cited above provides the instant invention as defined in original claim 2. In particular, none of the references teach providing a master mask for providing an incomplete planar circuit and a slave mask having a pattern for completing the planar circuit and for correcting systematic errors induced by the master mask.

In US Pat. No. 6,818,3898 Fritze et al teach providing a first mask for forming dense features, a second mask for trimming the dense features to form trimmed patterns, and a third mask for interconnecting the trimmed patterns to form a circuit pattern. It is submitted that none of these three masks would be considered to be a slave mask having a pattern for completing the planar circuit and for correcting systematic errors induced by another mask. For example, the

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trim mask does not complete the planar circuit, but rather removes unwanted pattern features. In contrast, the interconnect mask does not correct systematic errors induced by either the dense feature mask or the trim mask. In fact, Fritze et al teach away from the instant invention as defined in original claim 2 by teaching that optical proximity correction and/or spatial frequency correction is to be provided by either the dense feature mask (e.g., claims 59,60) or the trim mask (e.g., claims 63, 64), rather than the interconnect mask (see column 9, lines 25-30).

In US. Pat. No. 7,08,596 Liu teaches using a set of masks (claims 25,26), which for example, includes a phase shift mask and a trim mask (column 2, lines 59-61). Liu does not teach providing a separate mask for completing the planar circuit, and thus cannot teach providing a slave mask having a pattern that completes the planar circuit and corrects systematic errors induced by the master mask.

Secondly, it is submitted that it would not be obvious to one having ordinary skill in the art to provide a master mask for providing an incomplete planar circuit and a slave mask having a pattern for completing the planar circuit and for correcting systematic errors induced by the master mask, in view of the cited prior art. In particular, both Fritze et al. and Liu disclose using optical proximity corrections (OPCs). Referring to column 9, lines 15-30 in Fritze et al., OPC is used at the source of the problem to predistort the pattern such that the exposed final feature resembles the desired feature. This teaches away from the invention defined in original claim 2, wherein the slave mask provides part of

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the circuit that was not originally present (i.e., for completing the planar circuit) to correct systematic errors in the incomplete planar circuit (i.e., induced by the master mask). Providing a master mask for forming an incomplete planar circuit and a slave mask for completing the planar circuit and correcting systematic errors induced by the master mask has a number of advantages. For example, as discussed in paragraph [14] of the instant application, this means that only a small portion of a planar circuit needs to be redesigned and/or rewritten to provide the corrections (i.e., as opposed prior art OPCs, wherein most of the circuit needs to be redesigned). Accordingly, the mask set defined in original claim 2 can be used to provide a simple, efficient, and cost effective method for optimizing planar circuits.

Moreover, the rejection of original claim 3 is respectfully traversed. In particular, it is submitted that none of the references disclose an experimentally optimized second pattern. In fact, Fritze et al and Liu teach away from the instant invention defined in claim 3 by using OPC, which determines the corrections based on simulations. Using a slave mask that has been experimentally optimized allows a user to compensate for the fact that optical properties of planar circuits are not typically uniform over the entire wafer (e.g., as discussed in paragraph 10 of the instant application).

Furthermore, the rejection of original claim 4 is respectfully traversed. In particular, it is further submitted that none of the cited references, or combinations thereof, disclose providing a master mask having a first pattern with a

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featureless region and a slave mask having a perimeter with the same shape and dimensions as the featureless region. As discussed in paragraph [64] of the instant application, providing a slave mask with the same dimensions as the featureless region allows the second pattern to be seamlessly stitched to the first pattern to provide a complete optimized planar circuit. More specifically, it allows the smaller second pattern used to correct systematic errors to be positioned and stitched within the larger first pattern.

In view of the foregoing arguments, it is respectfully submitted that claims 2, 3, and 4, which depend from amended claim 1, also include allowable subject matter.

Claims 1, 9, 10, 12, 15, and 19-33 have been amended to specify that the planar circuit is a planar lightwave circuit. An example of support for this subject matter includes original claim 12. No new subject matter has been added.

Claims 9 and 35 have been amended to provide consistency between the preambles and the body of the claims and to correct antecedent errors resulting from the amendment of claim 1.

Claim 21 has been amended to specify that the at least one modificator section is designed for tuning the planar lightwave circuit. Some examples of support for this subject matter are found in paragraph [59] and [73]. No new subject matter has been added.

Claims 22, 27, 28, and 33 have been amended to correct dependencies.

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New claim 36 has been added. New claim 36 specifies that the first pattern is for providing a general layout of the planar lightwave circuit, and that the features in the second pattern are for tuning the planar lightwave circuit. New claim 36 is dependent on claim 1, and hence is believed to be both allowable and part of elected Group 1 (Claims 1-8). Some examples of support for this subject matter are found in paragraph [59] and [73]. No new subject matter has been introduced.

Figure 1 has been amended to include the legend -Prior Art-. No new matter has been introduced.

Early and favorable reconsideration of the Examiner's objections is respectfully requested.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 50-1465 and please credit any excess fees to such deposit account.

Respectfully submitted,

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